A DC ERROR AMPLIFIER FOR AN ANALOG-TO-DIGITAL CONVERTER

EUGENE J. REIHER

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Submitted in partial fulfillment of
the requirements for the degree of

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ABSTRACT

A brief resume' of contemporary Analog-to-Digital Converters with particular emphasis on the Voltage-Comparison method is given. Criteria for selection of a transistorized DC error amplifier for such a system are discussed and the more common types listed. In order to escape the severe drift problems of the DC amplifier, the use of two AC amplifiers in parallel to cover the frequency spectrum desired is investigated. One amplifier passes frequencies from several cycles per second to the upper limit desired; the second passes frequencies from DC to several cycles per second, with the aid of a chopper. A DC amplifier as described above was designed, constructed and tested for frequency response, with results which demonstrate that such a system is feasible. Recommendations for further development, including the use of transistor choppers, are presented.

The work for this thesis was done at Cubic Corporation, San Diego, California during the period from 20 January through 24 March 1958 and at the U. S. Naval Postgraduate School, Monterey, California from 31 March to 15 May 1958. I wish to express my sincere appreciation for the guidance given me by Professor Mitchell Cotton and Professor Abraham Sheingold of the U. S. Naval Postgraduate School, and to Sam Levy and Alex Bernstein of Cubic Corporation for their helpful suggestions and assistance.

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TABLE OF SYMBOLS AND ABBREVIATIONS

DC	Direct current
AC	Alternating current
ADCON	Analog-to-Digital Converter
DACON	Digital-to-Analog Converter
Bit	Binary digit
A	Voltage Gain
FF	Flip-Flop
V_{ref}	The precision voltage which is applied to the summing network resistors
V_x	The unknown analog voltage level
PCM	Pulse Code Modulation
CRT	Cathode Ray Tube
KC	Kilocycle
MC	Megacycle
K Ω	1000 ohms
mv	millivolts
μ secs	microseconds
db	decibels
Ico	Collector current for zero emitter current
tr	rise time
fs	cutoff frequency of an ideal amplifier
fo	Frequency of unity gain

CHAPTER I

INTRODUCTION

A. Objective

In recent years, a useful and sorely needed technique has been developed to assist in the collection and evaluation of technical data. This technique is ADCON, Analog-to-Digital Conversion. The most apparent use for an ADCON is as a processing agent for analog, or continuously varying, data which is to be analyzed by an electronic digital computer. A second important usage occurs in the field of radio telemetry. Information collected in a test vehicle, say a rocket, generally modulates a carrier frequency which is then transmitted to a remote receiver. If the modulation is PCM, the deterioration of data accuracy is significantly reduced because of the relative ease of determining the presence or absence of a pulse [1]. The object of this paper is to describe and discuss a DC amplifier which has been designed for use with one particular type of ADCON, the Voltage-Comparison Encoder. To provide background for the development of this project, a brief discussion of the three major types of ADCONs is given. Considerable attention is given in Chapter II to the logic associated with the Voltage-Comparison encoder and the DC Amplifier is shown to be the heart of the system.

B. Major types of ADCONs

Although many variations have been used [2,3,4], three

general types of ADCONs predominate. These are the Time encoder, Spatial encoder, and the Voltage-Comparison, or Feedback, encoder. The operating principles of each will be described briefly.

1. Time encoder.

In this system, a linear sawtooth and the unknown voltage are sent to a comparator. When the sawtooth passes through zero, a counter is started. This counter is stopped when the comparator indicates that the sawtooth and the unknown are equal in magnitude. Thus the number of pulses counted is a representation in binary form of the unknown voltage.

2. Spatial encoder.

The unknown here may be either an angular shaft position or a voltage level. For the latter condition, the unknown voltage level is connected to the vertical deflection plates of a masked cathode ray tube. For each voltage level, a corresponding horizontal line on the face of the CRT is masked in such a manner that a binary code representing the level is presented for read out to photocell circuitry. The horizontal line may be illuminated by using a conventional sweep or by flashing a thin horizontally orientated wafer of electrons from the gun. Shaft position encoding is similar except that a light source, slit, and radial mask are used, no CRT being necessary.

3. Voltage-comparison encoder.

Basic to this method is the sequential sub-

traction from the unknown voltage of a series of precision voltages, each one half the magnitude of its predecessor. After each subtraction, the most recent subtrahend is retained if the difference is greater than zero, and is removed if the difference becomes negative. When the smallest precision voltage has been subtracted, the states of a series of flip-flops associated with each precision voltage may be read out as a binary representation of the unknown voltage. The logic circuitry is then reset to repeat the cycle on the next unknown input sample.

C. Comparison of ADCON types

If a high sampling rate is the major consideration, the SPATIAL encoder is best, attaining sampling rates to 10 MC at .1% accuracy. The chief accuracy limitations are the beam width of the CRT and the linearity of the vertical deflection circuitry. While the circuits are simple, a high volume of auxiliary equipment is needed. Because of the CRT, this encoder is not particularly suitable when extreme shock and vibration are expected.

For the best precision, a time encoder should be chosen. Accuracy is limited by the sweep linearity and the sensitivity of the comparator. The sampling rate is slower than the other methods. With optimum flip-flop speed in the counter (10^7 pulses/second) and .1% resolution, the maximum sampling rate is 10,000 samples/second.

A compromise between the two types is the Voltage-

Comparison encoder. Using .1% resolution, rates of over 100,000 samples/second may be attained. Speed is limited by the speed of the counter and by switching speed in the logic net. Accuracy depends upon the precision voltages and resistors used in the comparison network and on the efficiency of the switching devices which apply and remove the precision voltages. About .1% accuracy is obtainable at the present time. The chief disadvantage of this method is that a considerable amount of logical circuitry is needed, but transistorization will allow the encoder to be encased in a reasonable volume while also keeping power requirements low. The object of my work at Cubic Corporation was to contribute to an analog-to-digital converter of the following specifications:

.1% Accuracy

Range -100 to +100 Volts

Transistor design (for ruggedness and low power and volume considerations)

Sampling Rate of about 50,000 pulses/second

It is apparent that these specifications fit the Voltage-Comparison encoder well; hence, this method was chosen.

CHAPTER II

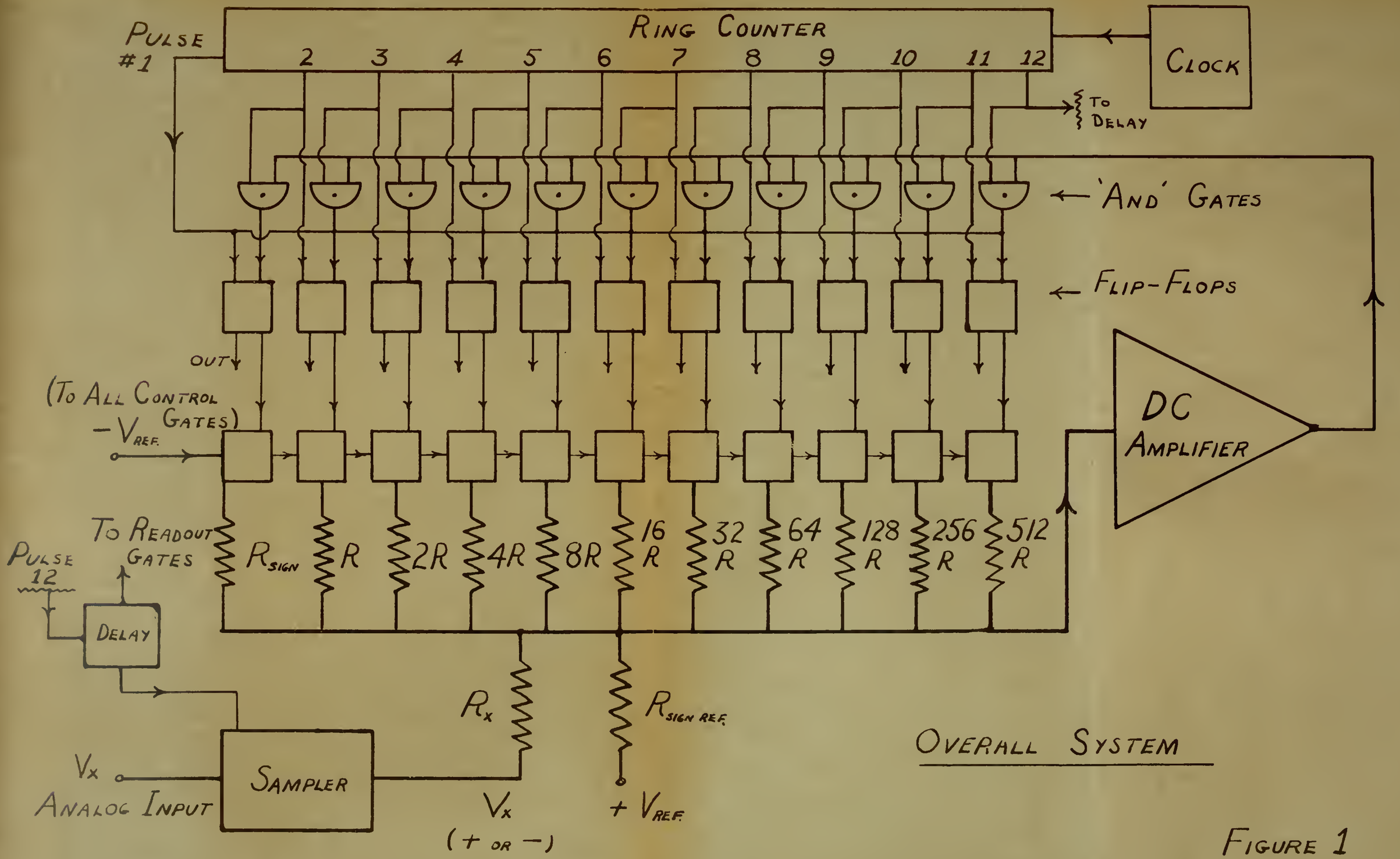
A VOLTAGE-COMPARISON ADCON

A. Block diagram.

The operation of the overall system may best be understood by referring to Figure 1. Clock and counter pulses are of positive polarity. The AND gates will conduct when a pulse from the counter is sent to them simultaneously with a positive enabling level from the DC amplifier. For the flip-flops, the set output is high when the flip-flop is set, and low when it is reset. Control gate j will apply $-V_{ref}$ to Rj when FLIP-FLOP j is set, and will ground Rj when FLIP-FLOP j is reset. The SAMPLER reads the level of the analog unknown and holds this level until the cycle of logic is completed. The delay device allows for parallel readout (from the RESET outputs of the flip-flops) and for the next sample to be taken after pulse #12 and before pulse #1 of the new cycle. This could just have well have been done by including pulse #13, but would have reduced the sampling rate slightly. R_{sign} and $R_{sign\ ref}$ are included as an offset factor to allow both + and - input voltages to be analyzed. For this system $R_{sign} = R_{sign\ ref} = R/2$.

B. Operation.

The sequence of operation begins with the sampler, having previously tested the unknown, holding a level V_x for the length of the cycle. Pulse #1 sets FF #1 and resets



Overall System

Figure 1

all others. Thus $-V_{ref}$ is applied to R_{sign} while R, 2R, etc. are all grounded. Assuming the DC Amplifier input to be at a virtual ground, the polarity of the input signal will be the same as that of Vx. This is so because $+V_{ref}$ is equal in magnitude to $-V_{ref}$, and effects a temporary cancellation. Assume Vx is +. Then V_{out} (of the amplifier) is - , inhibiting the passage of pulse #2 through AND gate #1. Thus $-V_{ref}$ remains applied to R_{sign} for the entire cycle. The effect is as if R_{sign} and $R_{sign\ ref}$ were not included in the system. If V_x were negative, however, the logic would ground R_{sign} for the remainder of the cycle. The system would then operate on $(+V_{ref} - V_x)$, a positive quantity. The reset output of FF #1 represents, therefore, the polarity of V_x, "low" being equivalent to + and "high" equivalent to -.

Assuming a positive V_x for illustrative purposes, we continue with pulse # 2. In addition to feeding AND gate # 1, pulse # 2 sets FF # 2. If $\frac{V_x}{R_x} > \frac{|V_{ref}|}{R}$, the net current flow will cause the input summing junction to be +. Since $R_x = R/2$, this may also be stated as $V_x > \frac{|V_{ref}|}{2}$. The logic will then cause no change in FF #2 when pulse # 3 arrives. This means that $\frac{|V_{ref}|}{2}$ has been subtracted from V_x. If $V_x < \frac{|V_{ref}|}{2}$, the DC Amplifier will have a -output and pulse # 3 will ground R. Pulse # 3 also applies $-V_{ref}$ to 2R. $\frac{|V_{ref}|}{4}$ is thereby subtracted from the remainder of the preceding decision (i.e. from either V_x or $V_x - \frac{V_{ref}}{2}$). Similar

logic prevails for the remaining stages through pulse # 12. The current applied to the amplifier input at this time is:

$$I \cong \frac{1}{R}\left\{ V_x - V_{ref} \sum_{j=1}^{10} \frac{1}{A_j 2^j} \right\} \qquad (1)$$

Where Aj = 0 or 1 depending on the logical operation described above. For negative values, V_x may be replaced by $(\not V_{ref} - V_x)$ in the above equation. This leads readily to the interesting fact that the output for negative V_x values is the one's complement of $\not V_x$. Appendix I contains an example of the operation for a particular numerical value.

The process is completed by a parallel readout of the RESET outputs of the flip-flops. At the same time, the next V_x value is sampled in anticipation of Pulse # 1 appearing for round two.

Operation of the CONTROL GATE circuitry is explained in Appendix II.

CHAPTER III

CRITERIA FOR THE SELECTION OF THE DC ERROR AMPLIFIER

A. Performance required

By their nature, direct-coupled amplifiers are ornery devices, the severe drift of the output current with change of temperature being particularly vexatious. Also present are the problems of other amplifier types - attaining sufficient gain, appropriate bandwidth, and stability. With the exception of the latter, which will be discussed in Chapter IV, each of these will now be considered in detail, stressing the application to the ADCON system. Tentative system requirements are that a 5 mv signal input should result in a 5 volt output to a 2.7 K load. Clock rate is to be 500 KC, allowing two μ secs for the accomplishment of each decision.

1. Gain-bandwidth considerations.

Although transistor amplifier gain is more aptly described in terms of current or power gain, it is more convenient to speak of the voltage gain for this particular case. Considering solely the ratio of output signal to minimum input signal, the gain requirement for an open loop circuit would be A = 1000 or 60 db. For an operational summing amplifier, equation (2) is valid only when the open loop gain is high. Typical amplifiers have gains between 500 and 50 M [6]. The higher the gain, of course, the better the approximation. For errors less than .1%, the open loop again should be 66 db or better for R_f=R (see Appendix III). For

$R_f < R$ the error becomes even smaller.

Since the analog range includes 100 volts, and since transister circuits operate at a lower level, a practical summing amplifier would have an R_f lower than R. This leads to an important distinction regarding the function of the DC amplifier. That is, is it necessary to have a true digital-to-analog converter within the ADCON, as was assumed by the simplified presentation of Chapter II? The answer depends on the intended use of the system. If it is a contemplated marketing the device with the added capability of having a separable DACON included, then E_{out} of the amplifier should be a true representation of the analog voltage corresponding to the state of the flip-flops. For the system being considered such a feature was not intended. Output of the DC Amplifier, therefore, need not be an enlarged replica of the input, but must show rather whether or not the input is plus or minus in polarity at various periodic instants of the decision cycle. Limiting, either within the amplifier or at the input, would be permissible, the smallest expected signal ($\not$ 5mv) driving the output sufficiently to enable the gates to the flip-flops. If the DACON feature were included, the smallest positive signal expected could be made to trip a comparator which would in turn enable the gates.

Consider now the effect of bandwidth on the signal output. Since the input signal will be similar to a series of pulses, each of two μsecs in duration, the desired amplifier

may be likened to a video amplifier. Assume uniform transmission from zero frequency to fs, with no transmission above fs. Also assume that the amplifier phase shift is proportional to frequency within this band and that no limiting occurs within the amplifier. If a rectangular pulse is applied to the input, two significant characteristics of the output must be examined. These are the rise time of the output and the condition that the output be generally of rectangular shape. It has been shown [7] that the time to rise to maximum value is given by:

$$tr = \frac{.805}{f_s}$$

and that a pulse output of good detail is obtained when:

$$f_s = \frac{2}{\text{pulse width}}$$

This leads readily to a pass band up to one MC for a two μsec pulse, which means a rise time of .8 μsecs. Since delays may be expected in the logic circuitry as well, it would seem reasonable that f_s be made at least one MC to allow settling of the circuitry before the next pulse from the ring counter appears. Naturally deterioration of the actual amplifier from the characteristics of the ideal amplifier will alter the response. In particular, the phase variation should be less than .5 radian from a linear characteristic in a frequency range of 167 KC [8]. These criteria would not apply to an amplifier which used limiting since they were developed for a linear situation. In the latter

instance, the recovery time of the saturated transistors must be short enough to allow proper operation of the logic every two 4 secs. One practical way to prevent excessive overdrive of the transistors would be to limit the input with junction diodes.

2. Drift requirements.

Before a DC amplifier can be useful in a particular system the problem of drift must be met and conquered. Drift is defined as a slow variation in output current due to causes other than input signal. Equivalent input drift is the signal input required to restore the output current to the value required for zero output. With these defined, let us examine the causes and effect of drift in a transistor amplifier.

Changes in supply voltage and changes in operating temperature are the principle causes of drift. Assuming that the former cause may be reduced sufficiently by regulated supplies and adequate warm-up time, we may concentrate on the temperature. Transistor parameters will vary with temperature, the most troublesome effects being caused by changes in Ico, the collector current for zero emitter current, and in the forward resistance of the emitter-to-base diode [9]. These and other transistor variations prove troublesome even when direct coupling is not used, and can shift the operating point to such a degree that amplification is completely lost [10]. Some form of

temperature compensation must be used in conjunction with proper bias design [11,12,13] . When direct coupling is used the problem is more acute since a slight change in the DC operating point of each stage is amplified and passed on to succeeding stages. The final stage may easily be driven to saturation or cutoff by a slight change in the first stage, even with no input signal. Considering this for the ADCON system where five mv is to provide a five-volt swing, the equivalent input drift must be less than five mv. As a reasonable criterion we may say that the equivalent input drift should be two mv or less.

B. Types of DC Amplifiers Generally Used.

1. Temperature-sensitive networks.

Temperature-sensitive networks such as those described by Shea [11] and Keonjian [12] utilize resistors, back-biased diodes and additional transistors to compensate for Ico change with temperature. Typically they may reduce output current drift to a value 1% of room temperature current in the range 0° to 50° Centigrade.

2. Chopper stabilized.

For chopper-stabilized DC amplifiers, a feedback resistor connected from output to input reflects any output drift. When the DC level of the input junction is other than zero, a chopper breaks the DC voltage into a square wave which is amplified by an AC amplifier, filtered back to DC, and sent to some point in the circuit which will

cause a correction signal to reduce the drift almost to neutralization. A filter between the input and the chopper insures that only DC and very low frequency components are passed to the AC amplifier. It also prevents any significant amount of current to be drawn from the input when the chopper contact is grounded. One method of feeding back the signal is given by Blecher [14] and uses a complementary series of input resistors, and one from the output, with the chopper amplifier to introduce a correction at the summing junction due to drift alone.

3. Differential input.

In this system feedback from the output is sent to a differentially connected input [15] . That is, the feedback is to the base of a transistor which shares an emitter resistor with the input transistor. Characteristics of these two transistors are usually matched so that parameter changes with temperature balance out. A combination of the differential method with chopper stabilization, albeit for vacuum tube circuitry, is given by Bradley and McCoy [16] .

4. Balanced systems.

By differentially connecting transistors in each stage and cascading the stages, DC amplification may be obtained while drift due to temperature change is balanced out. An illustration of this system, which also uses input limiting, is shown in [17] .

C. Proposed DC Error Amplifier.

1. Operation.

A basic change from the preceding types has been made in the amplifier developed during the course of this work, though many of the features of the chopper stabilized amplifier are evident. This change is that no direct coupling has been used, with the important result that changes of DC operating points are not amplified and coupled to following stages. A block diagram of the amplifier is given by Figure 2, and an idealized gain-frequency response by Figure 3. Both the main amplifier and the chopper amplifier are RC coupled except that there are no capacitors from the last stage of the main amplifier to the output. Point x connects through a resistor to the base of the last stage. Feedback resistor Rf, as before, is used to keep the summing junction input at a virtual ground. The chopper amplifier is used in parallel with the main amplifier rather than as a stabilizing influence. Referring to Figure 3, the chopper amplifier should pass frequencies from DC to a few cycles / sec. The main amplifier must extend quite low in frequency, picking up where the chopper amplifier left off and continuing to the desired frequency fs. Addition of the two responses should produce a response approximately linear from DC to f_s.

The mechanical chopper runs at 400 cycles alternately grounding the input and output of the chopper amplifier. Thus a small DC signal at the input summing junc-

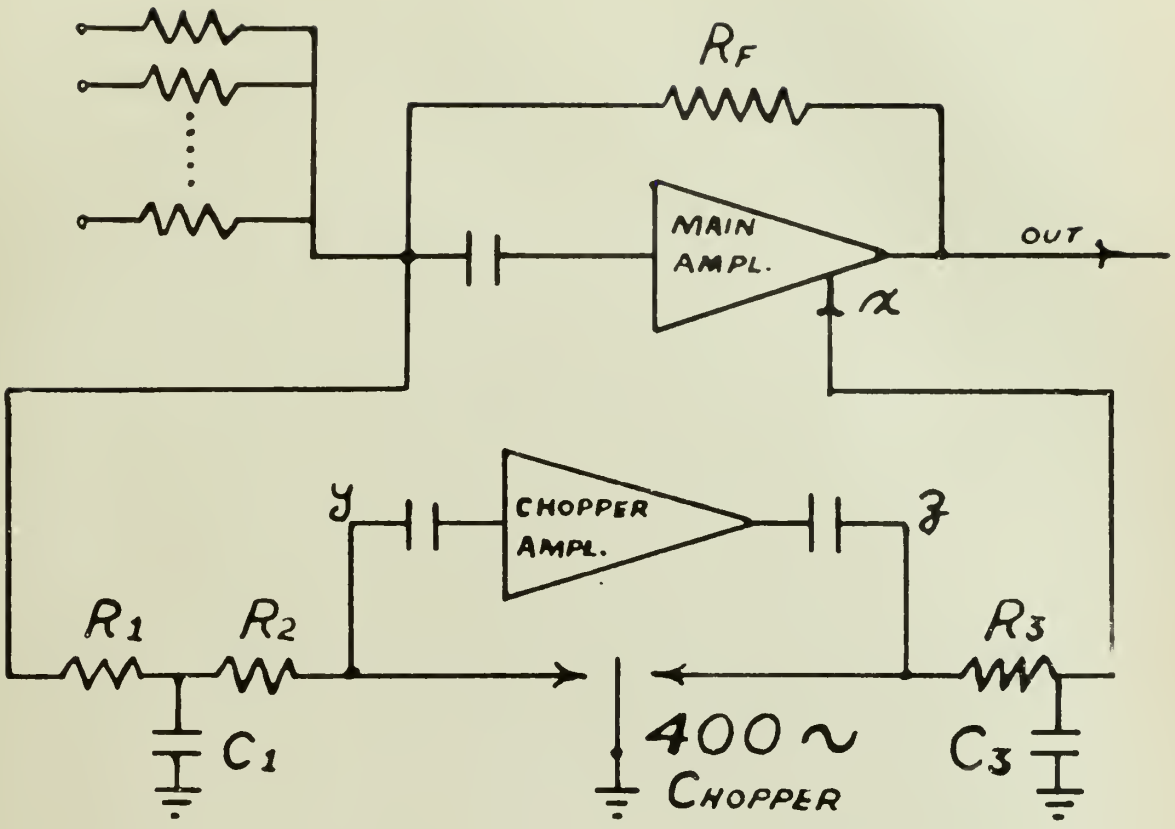


FIGURE 2. CHOPPER STABILIZED AMPLIFIER

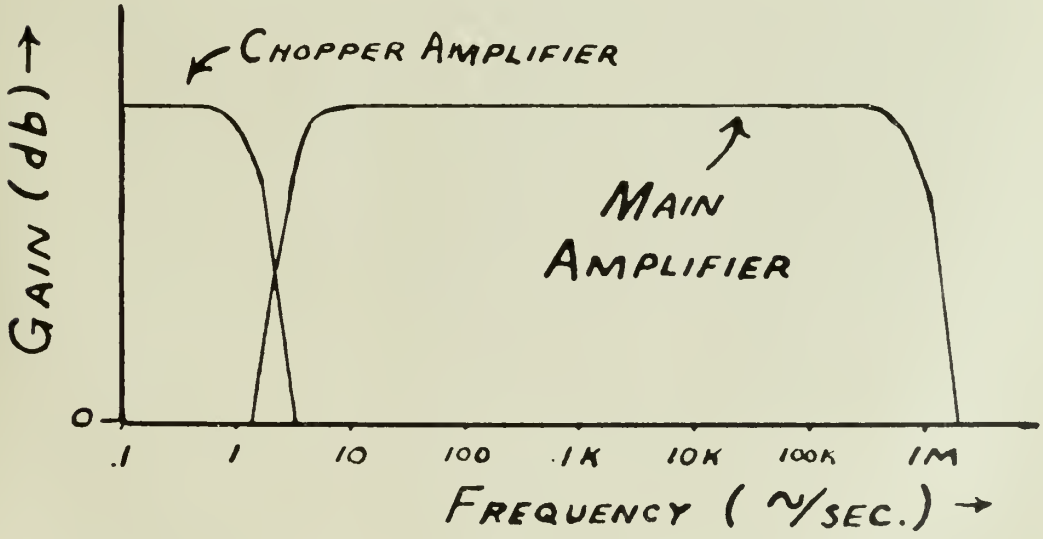


FIGURE 3. IDEALIZED RESPONSE CURVES

tion becomes, at point y, a square wave of the same polarity as the DC signal and clamped to ground. Since the chopper amplifier has a phase inversion and since point z is clamped when point y is not, the filtered output is of the same polarity as the original signal. This is illustrated by Figure 4. R_1C_1 and R_3C_3 are the input and output filters, respectively. Note that with the summing junction being maintained at a virtual ground, current flow through R_1 when point y is grounded by the chopper contact would be very small. Resistor R_2 reduces this flow even further.

2. Comparison with other types.

If this type of amplifier can be successfully substituted in this application for the more prevalent

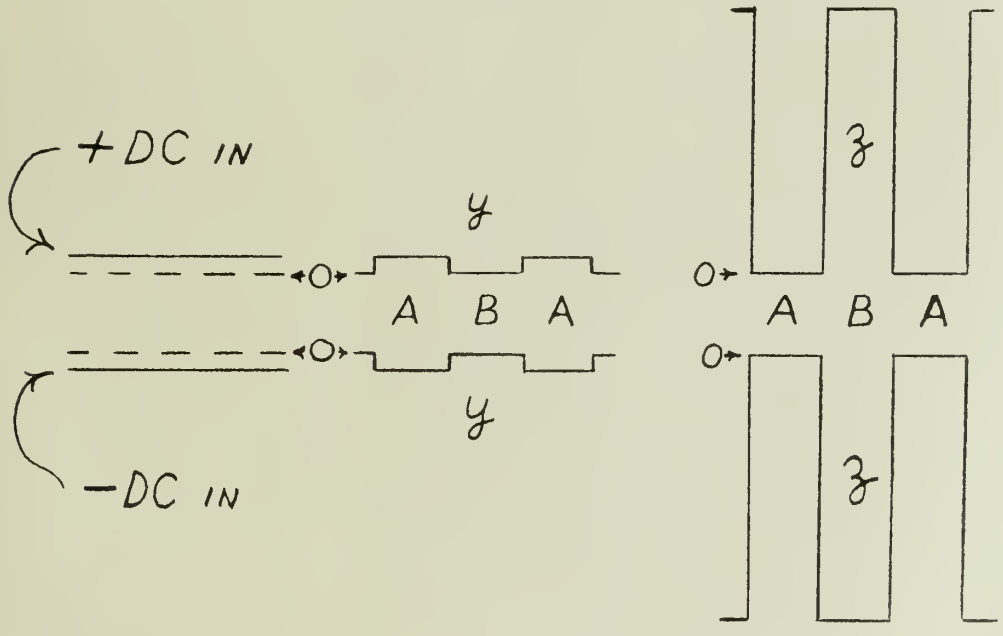


FIGURE 4. CHOPPER WAVEFORMS

direct-coupled amplifier, the major limitation of DC Amplifiers, successive amplification of DC operating point drift, will be avoided. Furthermore, the effect of the change of the emitter-to-base diode resistance with temperature may be minimized by insertion of a swamping resistor in the emitter leg, bypassed by a capacitor. For direct-coupled circuits, this capacitor could not be used because it would charge to the DC average of the imposed signal, producing a DC error in the output. Thus any emitter resistor used for swamping would also introduce degenerative signal feedback. For the proposed amplifier, biasing should be such that the operating point is on the linear portion of the characteristics. If extreme temperature variations are expected, temperature sensitive elements will probably be needed, as in any AC amplifier, to keep operating point shift small. With these precautions, the most likely cause of trouble would be the final stage which is direct coupled to the output. The feedback resistor will help minimize this drift, but will not be as effective as in the chopper stabilized case. Also, the emitter resistor for this last stage cannot be bypassed, but if the first two stages have sufficient gain this problem should not be too troublesome.

Of course, variation in the precision voltages for any reason, or in the relative resistances of the precision resistors with temperature, will produce an error output which is indistinguishable from the signal. This error is not a

function of the amplifier's characteristics, however, and would appear equally for any of the types mentioned. One obvious difficulty will be to match the frequency responses of the chopper amplifier and the main amplifier so that all frequencies lower than fs will be amplified approximately the same amount. It should be noted, however, that the gain need not be level to within .1% in order to attain that accuracy from the system, because of the manner in which the gain enters the equation of a summing amplifier.

D. Comparison of chopper types.

1. Mechanical choppers

The use of mechanical choppers to amplify low level DC signals is a long-established technique. In the conventional system a low-level DC voltage is mechanically chopped prior to amplification by an AC amplifier, and then filtered back to DC. Thus the relatively poor zero stability[1] and gain stability[2] of DC amplifiers is avoided. One such system developed by Williams, Tarpley, and Clark [18] uses this method for zero stability, combined with feedback for gain stability. The bandwidth available for such a system is low - much below the frequency of the mechanical chopper.

[1]Zero stability may be defined as the maintenance of zero output for zero input.

[2]Gain stability, as used here, is the maintenance of a constant gain as fluctuations of line voltage, temperature, and other disturbances occur.

Goldberg devised means of using the chopper in such a way that this bandwidth restriction is eliminated [19] . This method is the Chopper-Stabilized DC Amplifier discussed in III - B of this paper. An important advantage of the mechanical chopper for the latter system, and for the system of this paper, is that synchronous filtering is so easily obtained. By this is meant the mechanical clamping of input and output 400 cycle waves to ground to give eventually an amplified DC signal of the same polarity as the input. The errors at the summing junction due to the chopper itself, such as thermal emf caused by contact potential, are small (less than one mv), and the circuitry associated with the chopper is simple, i.e., the driving circuit. Disadvantages are high driving power, susceptance to vibration and shock, short lifetime (1000 hours), necessity of shielding between driving source and the chopper amplifier, narrow operating frequency range, and high cost.

2. Electronic choppers

In recent years electronic choppers have been developed using magnetic amplifiers, magnetic converters [20] , or switching transistors. A typical transistor chopper, using two npn transistors is described by Kruper [21] . Referring to Figure 5, a square wave control signal is applied through a transformer to the base of two transistors, alternately cutting one off while the other is switched on. The DC signal, of either polarity, causes

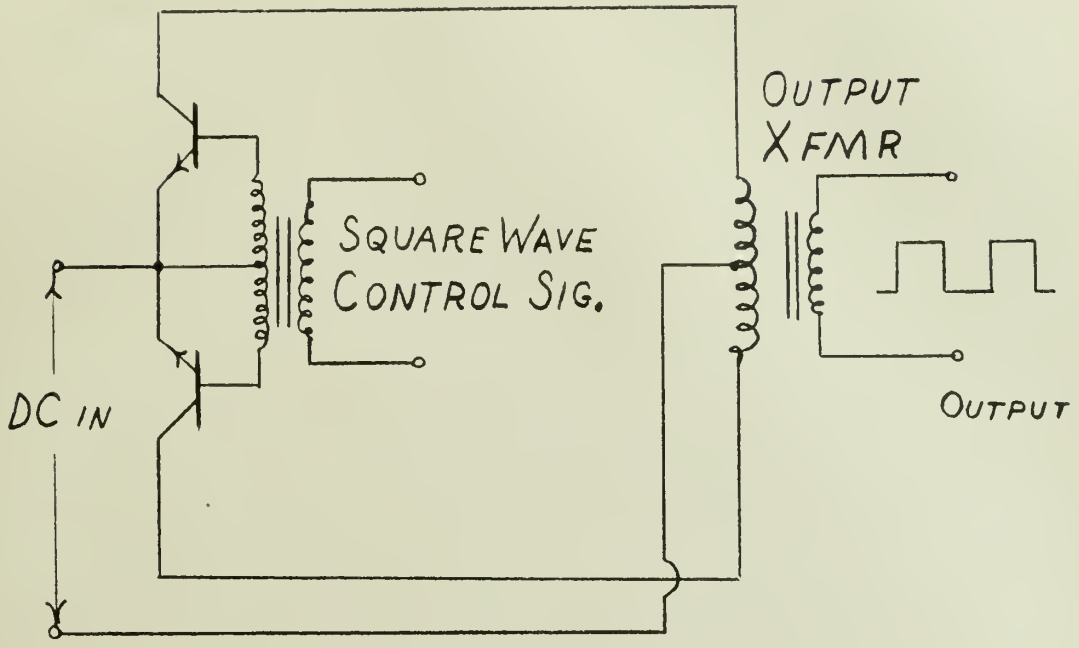


FIGURE 5. A TRANSISTOR CHOPPER

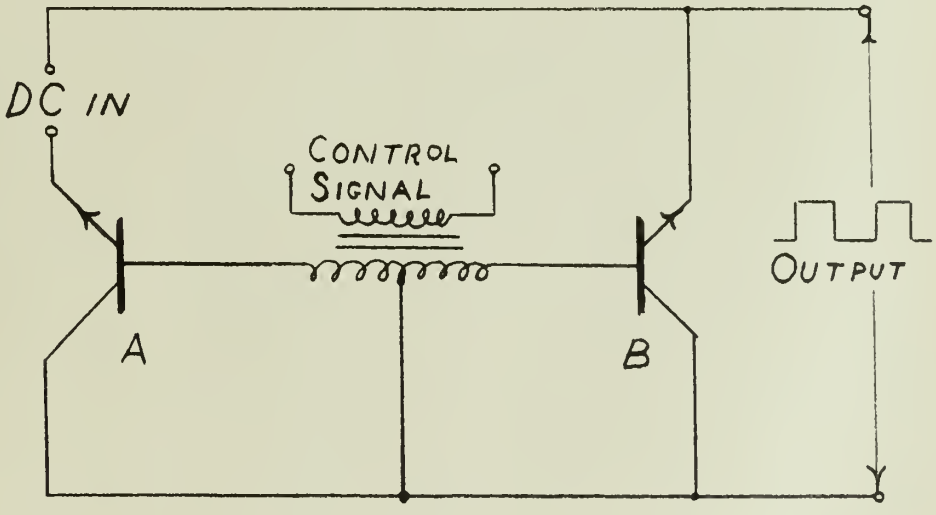


FIGURE 6. A TRANSISTOR CHOPPER WITH IMPROVED ZERO STABILITY

current to flow through that part of the output transformer which is in series with the conducting transistor. On the next half cycle the opposite transistor and output transformer-half pass current, producing a square-wave output which may then be amplified. This device does not act as an automatic clamp, as did the mechanical chopper of III - C. Therefore, the output of the AC amplifier must be synchronously filtered so that the polarity of the input signal is not lost. Another important consideration is the output obtained for zero input. Ideal switching characteristics for each transistor would have operation along the Vc- Ic axes, the voltage axis representing an open circuit and the current axis a closed circuit. For zero DC signal the load line would intersect the origin and no output would result. The actual characteristics are somewhat off this ideal, intersecting in the first quadrant just off the axis. Thus the zero signal load line through the origin produces a small error voltage. For the connection shown this error is over 10 mv. If the transistors are inverted (collector used as emitter and vice versa) the intersection is an order of magnitude closer to the origin, giving errors around 1 mv [22]. An adaptation of this circuit which eliminates this error voltage is shown in Figure 6. The basic operation is similar, the DC voltage being applied to the load when A conducts, and a short circuit appearing across the load when B conducts. The important difference is that the error voltage

for zero DC signal is applied to the load in the same direction for both A conducting and B conducting conditions. Then if the transistors are matched, the error is a DC error which does not pass to the AC amplifier. In both of the preceding circuits the input source resistance should be low to minimize any error due to the small transistor current flow through this resistor.

A third type of solid state chopper shown in Figure 7 is the ring bridge modulator described by Moody [23] . Referring to Figure 7, the control signal alternately activates paths XYZ and XWZ. The DC signal current flows through one

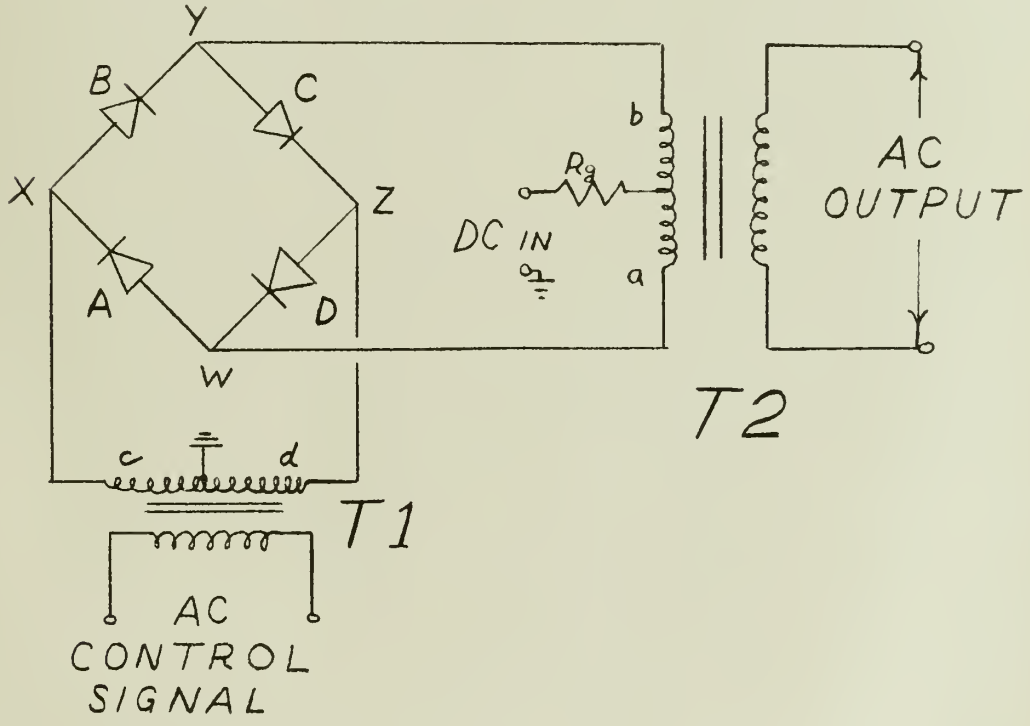


FIGURE 7. A RING BRIDGE MODULATOR

half of T2 to points X and Z through the activated path. Opposite and equal signal currents thus flow through the two halves of T1 producing no effect here. On the next half cycle signal current flows through the other half of T2, producing a square-wave output.

3. Comparison of Choppers.

Sensitivity of the mechanical chopper and the magnetic converter can be made as low as 10^{-9} amperes. The ring bridge modulator and transistor choppers have slightly higher sensitivities, but would do just as well for this type of DC amplifier. The latter two types have the advantage of ruggedness, low power, long life, shock and vibration resistance, small volume and weight, and the ability to operate at higher frequencies. The magnetic converter requires more power and is somewhat bulky. Advantages and disadvantages of the mechanical chopper have been mentioned in paragraph one.

The question arises, which chopper would be best for the DC Amplifier of III - C? Selection of the mechanical chopper was made at the time of designing the DC Amplifier because it was readily available and because of the ease of synchronized filtering when using it. The final choice must rest on the proposed use of the ADCON system. For example, if the system were part of an earth satellite, the average 1000-hour life of the mechanical chopper would make it an impractical choice. For guided missiles, this chopper would

be acceptable if the shock and vibrations expected would have no adverse effects, and if too large a percentage of its expected life were not used up in pre-firing tests. For ground installations the mechanical chopper is suitable provided that 1000 hours of operation is worth the forty dollars or so that the chopper costs.

Offhand the transistor choppers would seem to have the edge. One major drawback is the requirement that the source input impedance be low. This system must use a filter to restrict the chopper input to DC and low frequencies. The filter resistor, then, is a high impedance and must be considered a part of the input impedance. A second and less important disadvantage is that the transistor choppers need additional circuitry to accomplish the synchronous filtering of the amplified square wave. In view of these factors, and the time available for the project, choice of the mechanical chopper for this initial investigation seems to have been a fortunate one.

CHAPTER IV

THE DC AMPLIFIER

A. Chopper amplifier design.

1. Chopper amplifier.

Both the chopper amplifier and the main amplifier are outgrowths of the same basic design, the original intent being to build a universal package which could be used wherever an AC amplifier is needed in the system. It was soon noted that the different demands of the two amplifiers were not compatible, causing the design of each to diverge toward its own requirements. For the chopper amplifier the principle characteristic is that a 400 cycle square wave be amplified. Furthermore, the amplifier should be insensitive to low frequencies, less than ten cycles or so, since they are to pass only as a modulation of the 400 cycle carrier. The final circuit diagram is conventional in design and is given by Figure 8. The voltages were chosen the same as those of the main amplifier to keep power supply requirements to a minimum. Stages one and three use 2N123 pnp germanium transistors, stage two a 2N167 npn. Choice of an npn for the second stage was a carryover from an earlier attempt at direct coupling; a pnp could just as well have been used. The selection by transistor types was based on reasonably low Ico values (two μ amps average), and availability in stock. Voltage gain for 400 cycles was measured at 64db. Approximate bandwidth between three db points for the chopper

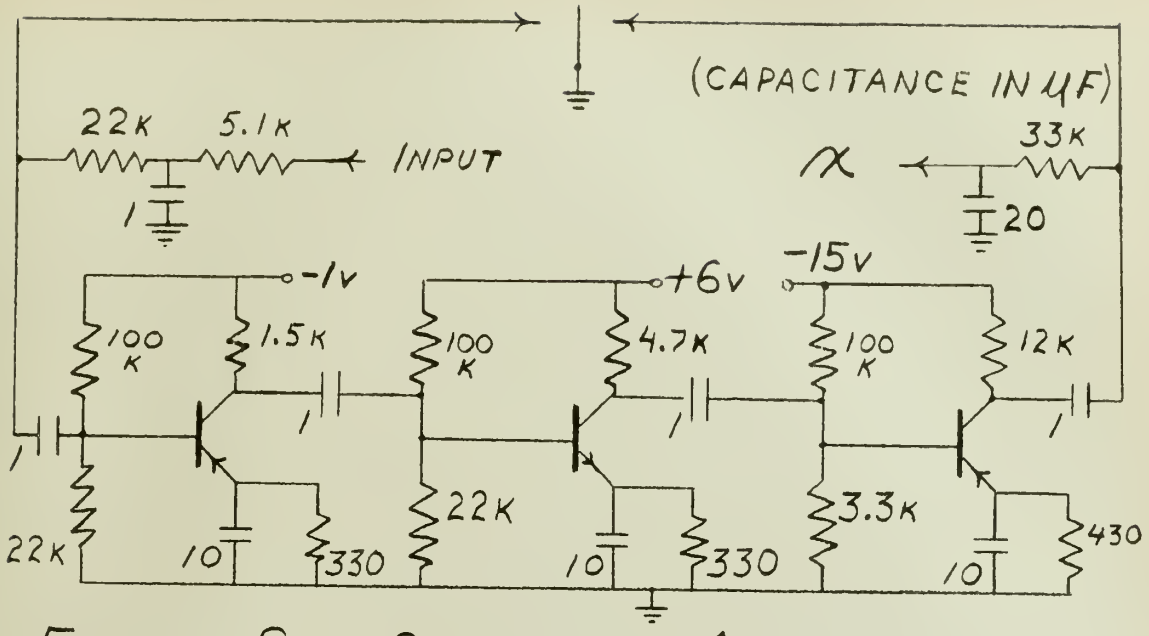


FIGURE 8. CHOPPER AMPLIFIER

amplifier alone was from 300 cycles to seven KC. A signal of six mv peak-to-peak drives the amplifier to saturation at 400 cycles.

2. Chopper.

The mechanical chopper used was a Bristol Company Synchroverter switch, part number C1414. As in many choppers, the synchroverter has make-before-break contacts to prevent transient pickup during switching. Drive for the chopper coil is provided by a transistorized 400 cycle free running multivibrator, rather than 400 cycle AC, to simplify system power requirements.

3. Problems encountered.

a. Amplifier limiting.

As mentioned in paragraph one, the amplifier became saturated for 400 cycle/second signals of over six mv swing.

For the purpose of demonstrating the principle of complementary frequency response, this is satisfactory since the main amplifier also saturates at this approximate level for mid-frequency signals. A signal smaller than this value was used when taking the frequency response. For a system incorporating a DACON and working at the high voltage range of this one, the chopper amplifier would have to use higher supply voltages, and hence different transistors, to prevent saturation.

b. Stray pickup.

Stray wiring pickup from the multivibrator to the input to the chopper amplifier proved to be a major problem. Only the slightest trace of transient spikes at base one was sufficient to drive stage three into saturation, with the input summing junction grounded. This pickup was minimized by encasing the chopper, multivibrator, and filters inside a shielded box. Shielded cabling was used for all leads to and from the input filter as an added precaution. In another instance, severe 60 cycle pickup, primarily from the power supply, caused a 60 cycle/second output, chopped at a 400 cycle/second rate. If 60 cycle/second circuits are to be used near the chopper amplifier for a system of this type, unwanted response may be reduced by cutting off the low frequency response between 60 and 400 cycles/second, by using a 60 cycle/second trap, or by having the amplifier tuned to 400 cycles/second [24].

B. Main Amplifier Design

1. Main amplifier

Figure 9 is a circuit diagram of the main amplifier. Transistors are again 2N123 pnp for the first and third stages, and 2N167 npn for stage two. A closed-loop frequency response of this amplifier was taken and is presented as Figures 10a and b. High-valued emitter and coupling capacitors were used to extend the response to quite low frequencies, as indicated in the figure. Mid-frequency gain was 56 db and saturation was reached here with a six mv peak-to-peak input. The upper three db point occurred at about 100 kc, lower than the value of one MC recommended in paragraph III-A for a two μ sec pulse. Since transisterized wide-band AC amplifiers extending well above this frequency have been developed [25], the problem of extending the response upward is not severe. When the chopper circuit was used in conjunction with the main amplifier, no appreciable difference in gain was noticeable for frequencies above 1.5 cycles/second. The dotted curve of Figure 10a shows the response due to the chopper amplifier alone. Except for DC, no readings were taken below .2 cycles/second. Closed-loop gain for DC was measured at 34 db, lower than the value desired but sufficient to demonstrate the feasibility of using complementary amplifiers. Open-loop gain for DC was 60 db, a more encouraging figure.

2. Coupling from the Chopper Amplifier

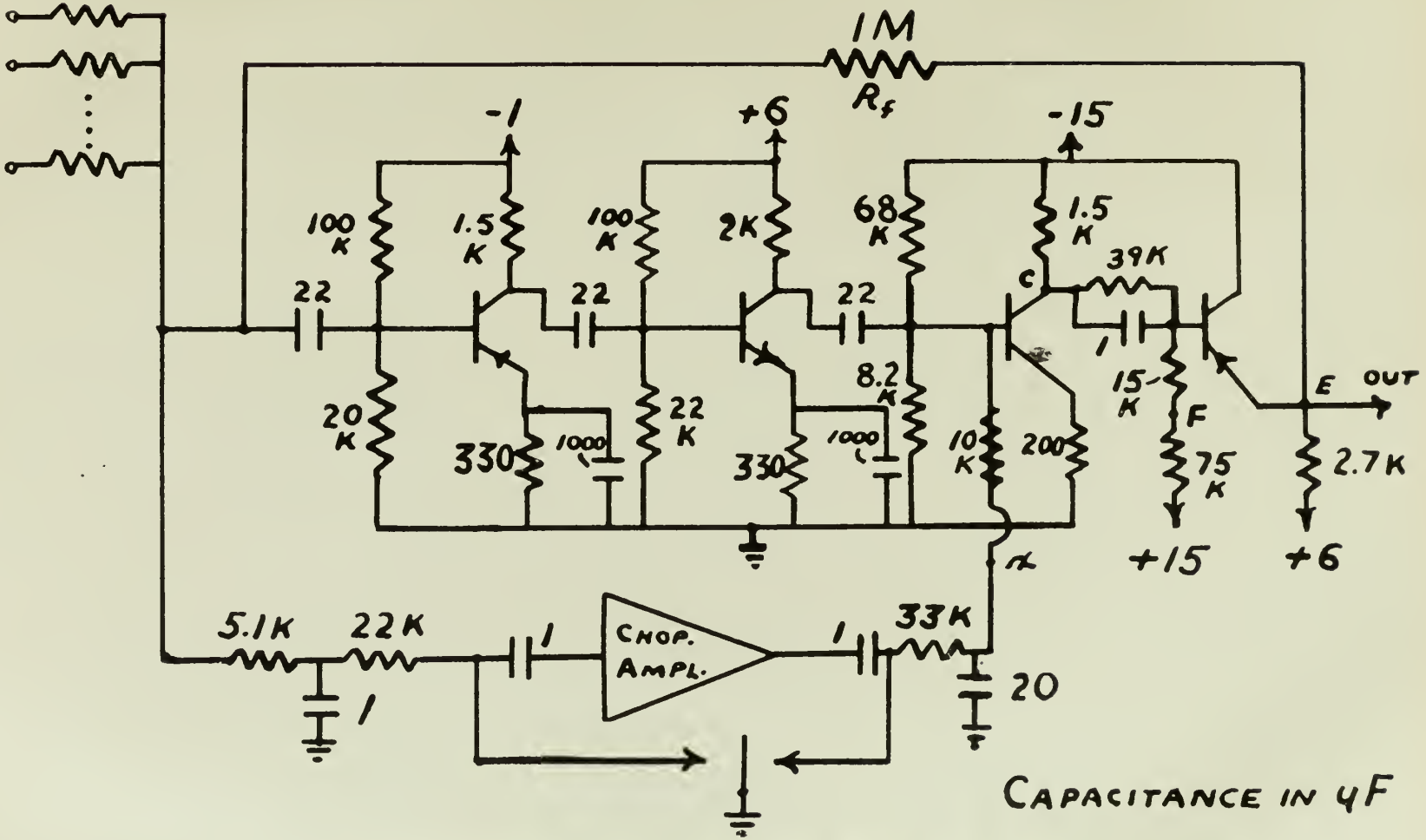


FIGURE 9. CIRCUIT DIAGRAM OF MAIN AMPLIFIER

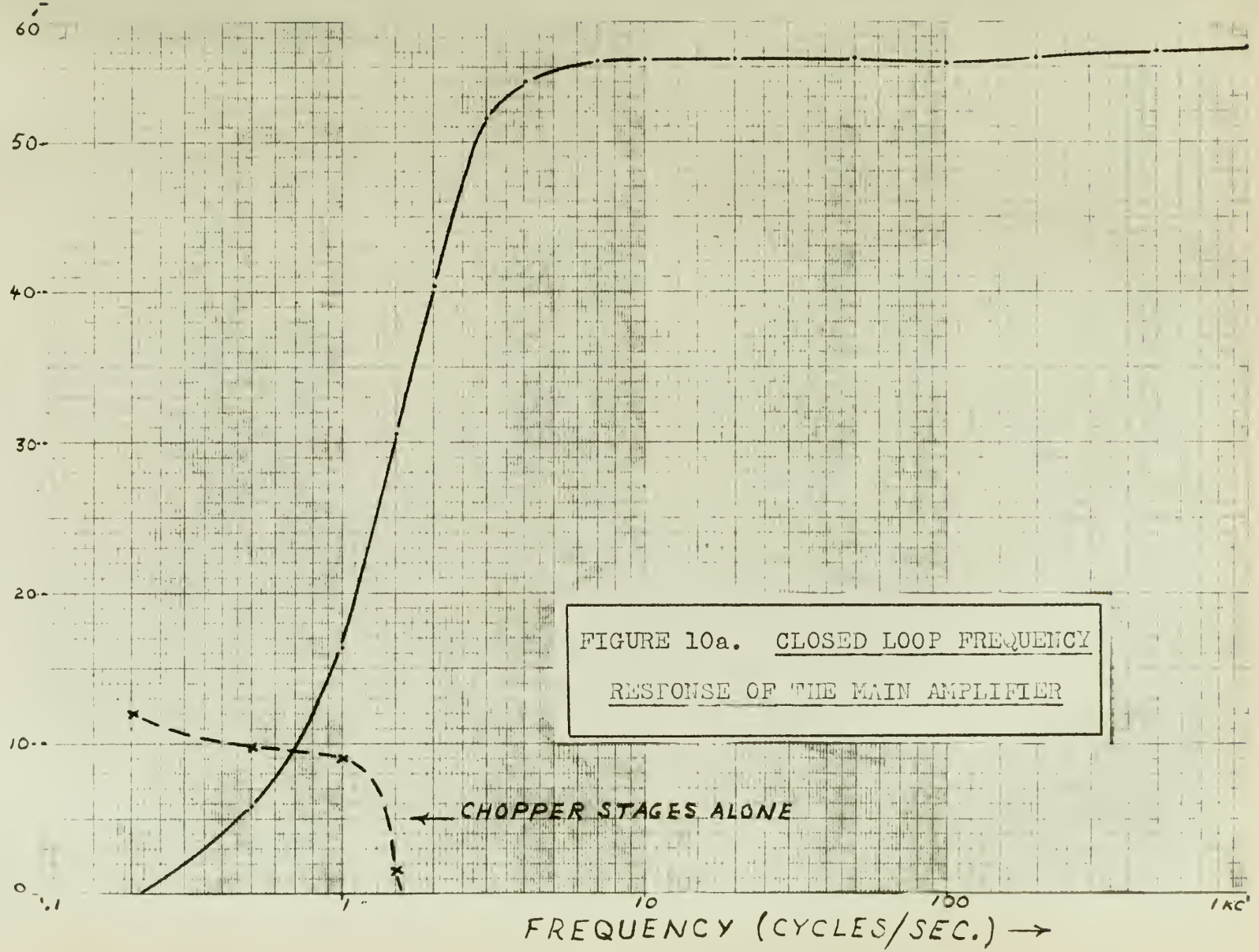


FIGURE 10a. CLOSED LOOP FREQUENCY RESPONSE OF THE MAIN AMPLIFIER

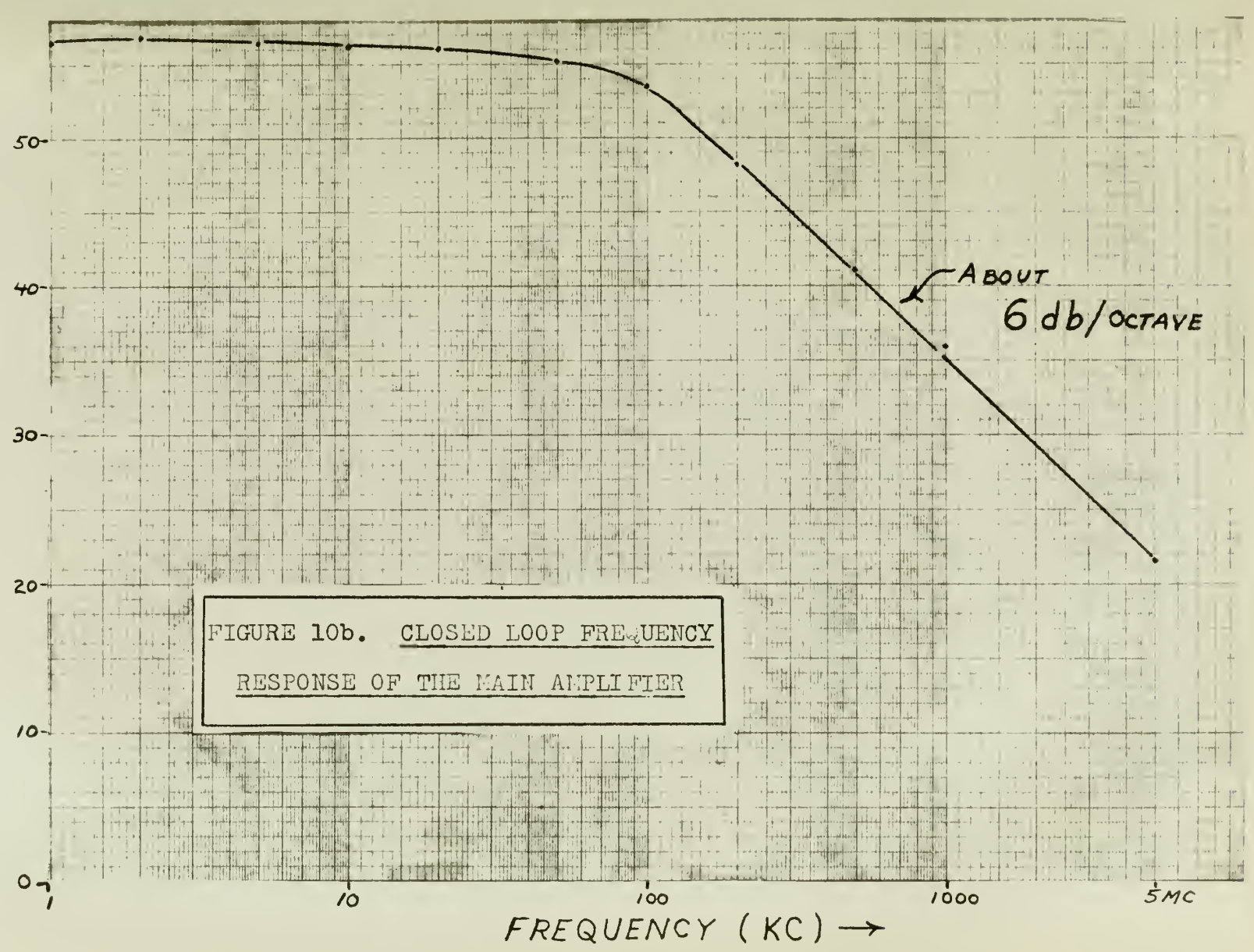


FIGURE 10b. CLOSED LOOP FREQUENCY RESPONSE OF THE MAIN AMPLIFIER

Several different methods of coupling were tried with that of Figure 9 settled upon. Omission of the 10 KΩ resistor would be satisfactory from a DC standpoint, but AC signals from stage two would be shorted to ground by the 20 μf filter capacitor.

Figure 11 shows an alternate approach. An emitter follower is inserted between the filter and the base of stage three. The input voltage divider must now return to a positive voltage to prevent cutoff of the emitter follower when the filter signal is positive. With the base of the third-stage transistor quiescently maintained at zero volts, emitter three also returns to a positive voltage. A value of 1.5 volts gives the collector of this transistor an operating point midway between saturation and cutoff for the resistance and voltage values used. If the emitter resistor is increased, a higher voltage could be used but excessive signal degeneration results. Because AC signals coming through the main amplifier were clipped at the base-emitter junction, in the absence of emitter bypass capacitors, it was felt that direct coupling from the filter was superior.

3. Output Circuit design.

Requirements of the output are that the feedback resistor should be at zero volts quiescently, and should be capable of positive and negative swings when the input changes minus and plus, respectively. The output which enables or inhibits the logic gates should swing between zero

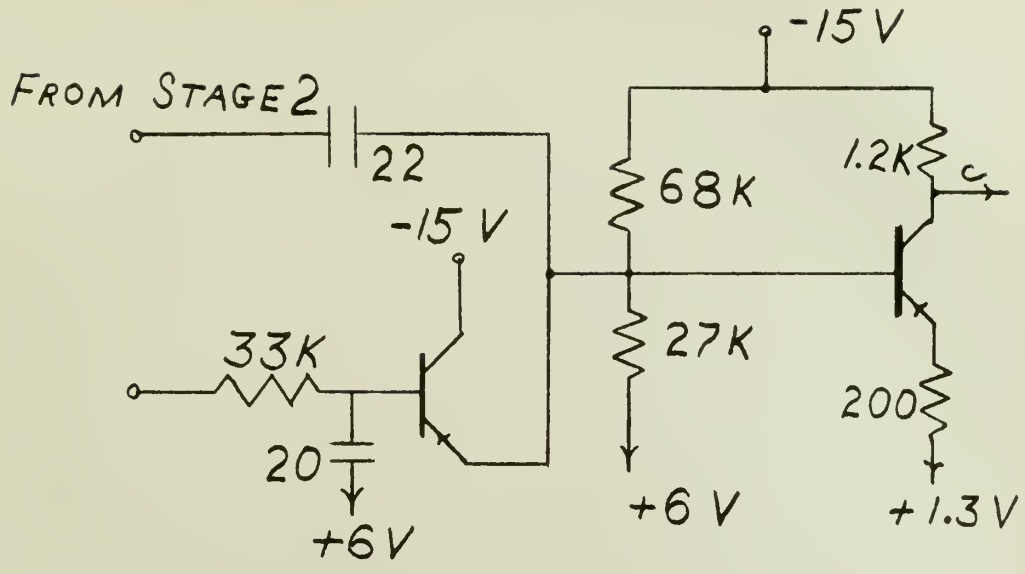


FIGURE 11. EMITTER FOLLOWER COUPLING

and ∕ five volts, if possible. To accomplish this, output to the AND gates should be taken from point F of Figure 9. An additional emitter follower, using a high current transistor, should be connected here to provide sufficient charging current for the AND gates without loading the amplifier excessively. If a full five volt swing is not available, point F may be moved closer to the ∕ 15 volt supply. Care must be taken that this voltage is not enough to enable the gates for zero signal condition, considering any expected power supply fluctuations.

4. Stabilization.

As with any amplifier, oscillations must not occur as the level of signals is changed. One indication of possible instability may be obtained from the plot of gain in

decibels versus log f. If the slope of the curve falls off at a rate greater than 10 db / octave near unity gain, possibility of instability occurs [26] . If the characteristics indicate this to be the case, interstage network shaping may be used to introduce a lead network. The corner frequency should be made lower than f_o, the frequency of unity gain, so that the rising six db / octave characteristic of the network will reduce the overall slope by this amount before, during, and for several db below unity gain. A more detailed, but complicated, frequency domain analysis of stability may be made by using Bode's return difference concepts. A thorough treatment of this method, applied to transistor amplifiers, has been published by Blecher [27] .

CHAPTER V

CONCLUSIONS

A. DC amplifiers.

The basic concept of using complementary AC amplifiers, one with a chopper, to produce wide-band DC amplification is sound, and development of an ADCON system around such an amplifier is feasible. An important decision which must be made prior to an ADCON's design is whether or not a separable DACON is to be included. For a specific industrial or military application, such as part of a guided missile, this seems unnecessary. On the other hand, if the ADCON is to be a general purpose commercial item, having a separable DACON provides an added touch of versatility, extending the range of usefulness of the unit. The DC amplifier, whether of the type discussed in this paper or another type, is affected by this decision. If a separable DACON is wanted, there must be no limiting in what will then be an operational amplifier. The AND gates will then be driven by a comparator following the amplifier, or possibly a DC error amplifier [28, 29] . If a separable DACON is not desired, this type of amplifier is still satisfactory; or one which limits the input signal may be used. For the latter case, it is recommended that the limiting be done at the summing junction. That is, the feedback resistor may be omitted and the summing junction returned to ground through a pair of junction diodes connected in parallel, plate to cathode. The forward resis-

tance of the diodes must be low enough compared to the lowest valued summing resistor to maintain the desired accuracy, and high enough to develop sufficient input signal. It should be realized that limiting within the amplifier when a feedback resistor is being used, does not really accomplish the purpose of the amplifier. Superficially it appears that as long as a positive or negative output indication is all that is needed, limiting does no harm. As pointed out by Johnson [30], however, limiting destroys the basis on which the operational amplifier equations were derived. That is, $E_{out} \neq -E_{in} A$. Because of this, the summing junction is not maintained at a virtual ground and the input signals are in error. The amplifier described in this paper, for instance, will work with the system as described in Chapter II only for low input signals below the saturation level. It can be made to work under signal-limiting conditions, however, by modifying the ADCON system as previously described in this paragraph.

B. Summing junction.

If the system is to be capable of encoding unknown voltages from -100 to +100 volts, the feedback resistor will have to be about four times smaller than the smallest resistance in the precision network of Chapter II to bring E_{out} down to voltages compatible with transistor circuits. This makes the feedback resistor small since the smallest summing resistor is itself restricted in size by the requirement that

the largest resistor be 2^{10} as big. One solution is to reduce the input unknown voltage, by a fourth say, using an operational amplifier. The remainder of the system may then operate on this unknown. The voltage applied to the precision resistors would now be made 25 volts to accommodate the new scale. If this voltage is too low, however, error due to voltage drops in the diode switches becomes more significant. An alternate solution is recommended. Several different configurations for the summing network have been suggested and successfully used in other systems [31, 32] . These are generally ladder networks which are arranged so that precision voltages or currents are generated in accordance with the position of a series of electronic switches. The currents or voltages can be made to be in the progression 1, $\frac{1}{2}$, $\frac{1}{4}$.... as required, but using resistors which do not vary R, 2R, 4R.... Smith's system [33] , for example, uses only R and 2R values. Thus R may be made rather large to accommodate the high voltage range, and the feedback resistor may then be increased in size also.

C. Accuracy.

Ten - bit information implies a resolution of one part in 1024, and sets a limit on the accuracy of about $\pm$ .05%. The accuracy of the system can by no means be considered synonymous with the resolution, however. For a .1% accuracy with a ten-bit encoder the open loop gain of the amplifier should be greater than 66db. The resistors and

voltages of the precision summing network, the zero drift of the amplifier, and the analog sampling mechanism must be better than .1% in accuracy, as well. To help achieve this accuracy it is recommended that the precision resistors be of a non-conductively wound, wire-wound type, each with a trimmer. If possible, they should be mounted near each other on a common heat sink, since their relative values determine the precision.

D. The chopper.

The advantages and disadvantages of the various choppers have been covered in more detail in III-D. Although the mechanical chopper was suitable for the purposes of this preliminary investigation, transistor choppers are recommended for this type of amplifier because of their relatively low cost, long life, ruggedness, low power requirements, and small bulk. This is done with the reservation that some means of neutralizing the error caused by "on condition" transistor current through the filter resistor must first be developed.

E. Summary.

Using the complementary AC amplifiers, one amplifying a chopped DC signal, as a substitute for a DC amplifier is a technique which is feasible for ADCON and other applications. For best results from a system accepting signals from -100 to +100 volts, a scaled reduction of the input or the use of a ladder type network is recommended. Either an operational summing amplifier with over 66 db open loop gain

to be followed by a comparator/error amplifier, or an input-limited DC amplifier with no feedback resistor should be employed. The transistor chopper should replace the mechanical chopper if the major problem of "on condition" transistor current can be solved.

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APPENDIX I

REACTION OF THE ADCON TO A SAMPLE VOLTAGE

For a numerical illustration of the ADCON operation we refer to FIGURE 12. Here a feedback resistor, R_f, is shown across the DC Amplifier. $|V| = |V_{ref}| = 100$ VOLTS. E_{out} refers to the output of the DC Amplifier, and all resistances have been doubled (since the ratio is the same, no contradiction with Chapter II occurs here). Let $R = R_f$.

As in Analog computers, if the forward gain of the amplifier is high and the input current to the amplifier negligible, E_{out} is given by Korn and Korn [5]:

$$E_{out} \cong -\frac{R_f}{R}\left(V_x \pm V - V - \frac{V}{2} - \frac{V}{4} - \cdots - \frac{V}{1024}\right) \qquad (2)$$

when all of the resistors are connected to -V.

For this example, let $V_x = \pm 60$ Volts. For the first decision:

$$E_{out} \cong -\frac{R_f}{R}\left(\pm 60 \pm 100 - 100\right) = -60$$

Since E_{out} is - , no change occurs for FF #1 and the ± 100 and -100 Volts cancel for the remainder of the cycle. They will be omitted henceforth.

For the next step,

$$E_{out} \cong -\left(\pm 60 - \frac{100}{2}\right) = -10$$

Therefore, no change in FF #2.

Continuing,

$$E_{out} \cong -\left(\pm 60 - 50 - \frac{100}{4}\right) = \pm 15$$

Here, FF #3 removes 4R from the process.

Next,

$$E_{out} \cong -\left(\not{60} - 50 - 12.5\right) = \not{2.5}$$

and so forth,

FIGURE 13 lists some of the values which may be expected for typical inputs. The resolution of the system is $\frac{1}{1024}$ or a little better than .1%. Note that the number obtained is not a binary representation of the decimal system since weighting is 50, 25, 12.5, etc., rather than 64, 32, 16, etc. The resistors could be adjusted to the proper values to obtain the latter weighting, if desired. Under this condition, however, the resolution would be 1.28 times as great.

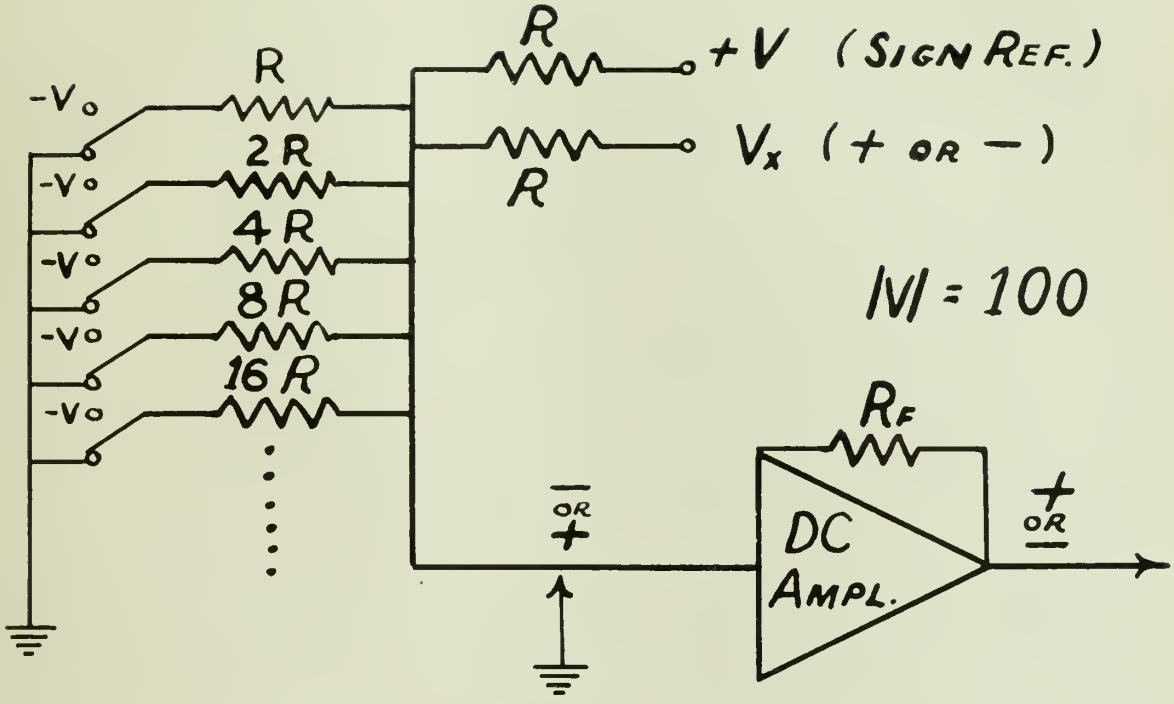

FIGURE 12 SIMPLIFIED SUMMING JUNCTION

V_x	SIGN	50	25	12.5	$\frac{100}{16}$	$\frac{100}{32}$	$\frac{100}{64}$	$\frac{100}{128}$	$\frac{100}{256}$	$\frac{100}{512}$	$\frac{100}{1024}$
+100	1	1	1	1	1	1	1	1	1	1	1
+60	1	1	0	0	1	1	0	0	1	1	0
0+ε	1	0	0	0	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	0	0	0	0
0-ε	0	1	1	1	1	1	1	1	1	1	0
-60	0	0	1	1	0	0	1	1	0	0	1
-100	0	0	0	0	0	0	0	0	0	0	0

FIGURE 13 TABLE OF TYPICAL VALUES

APPENDIX II

THE CONTROL GATES

The control gates which can be similar to the circuit shown in Figure 14, must use the non-regulated output of the flip-flops to apply or remove, as the logic dictates, a highly regulated voltage, V_r, to the associated precision resistors. To illustrate control gate action, let V_2 be $\nearrow$ 2 Volts and the flip-flop multivibrator signal be $\nearrow$ 5 Volts for the case where the flip-flop is set, and 0 Volts for the case where the flip-flop is reset. Assume R_{trim} is included in R_j. For the "set" condition, $\nearrow$ 5 Volts applied to the transistor's base will cut it off. Current flow will be as shown by the solid arrows, and diodes I and III will be back biased, provided $V_2' < V_3$. Since these are both negative voltages, this inequality occurs when

$$\left(\frac{R_b}{R_b \nearrow R_\ell}\right)|V_1| > \left(\frac{R_j}{R_j \nearrow R_a}\right)|V_r|$$

if the small diode voltage drops are neglected. This inequality should be designed into the circuit with sufficient safety margin to allow for changes in V_1 and for replacement of the transistor. The precision resistor for this stage would be $R_j \nearrow R_{trim} \nearrow R_A \nearrow R_{diode\ II}$.

For the "Reset" condition zero volts is applied to the base, allowing the current flow indicated by the dotted arrows. Assuming only a small V_{CE} for the transistor under this condition, V_2 and V_3 are at about $\nearrow$ 2 Volts, back-

biasing diodes II and IV. R_j is then grounded through R_B.

The diodes used in the system should have a low forward resistance and a high back resistance. Since $R_{\text{diode II}}$, the forward resistance of diode II, may be calibrated out of the problem by adjustment of R_{trim}, the forward resistance need not be an inescapable error. A high value of V_R, of course, also helps this situation. Care must be taken that the back resistances of I and III are very high. The effect of leakage current through these diodes may be studied by replacing them with their back resistances and drawing a Thevenin equivalent embracing V_1, R_L, R_B and the back-resistances in parallel with each other, loading the "ideal" circuit between R_A and R_{trim}. Several diodes in series replacing diode I, and a similar arrangement for III, will help keep the back-resistance high.

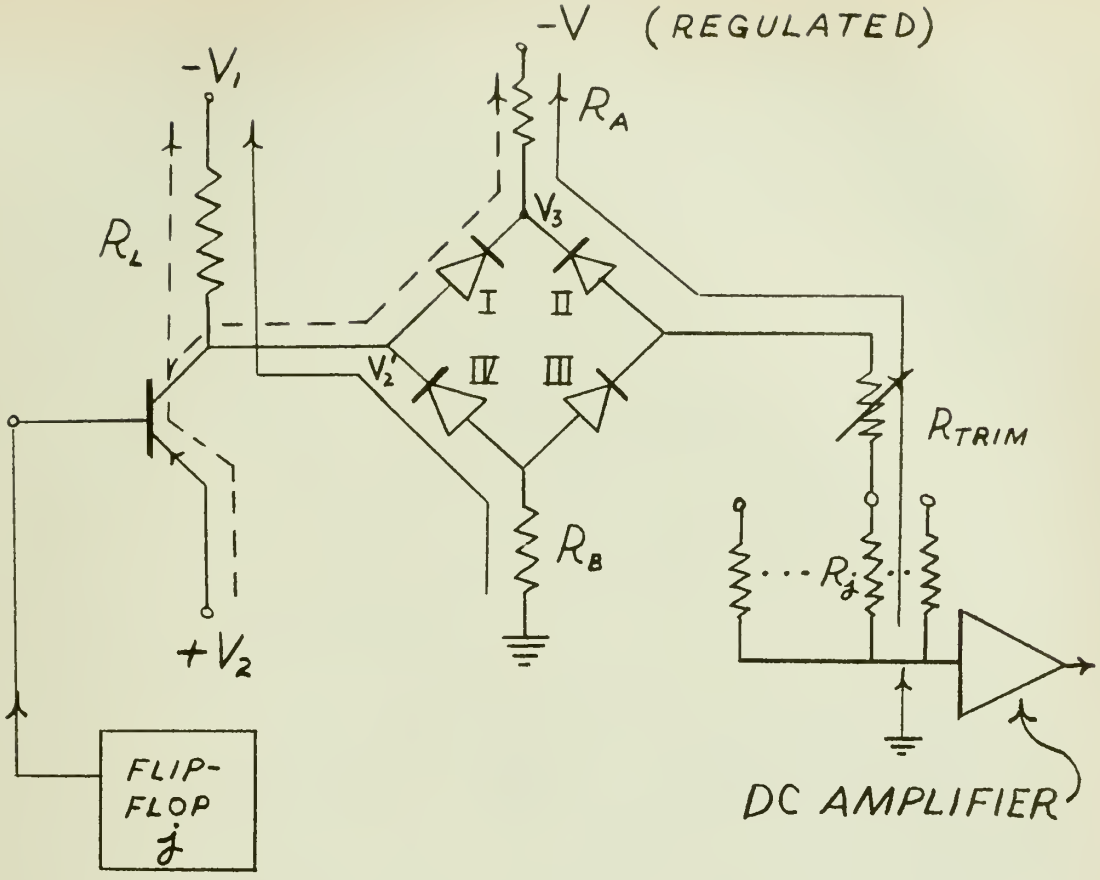

FIGURE 14. THE CONTROL GATE

APPENDIX III

SUMMING AMPLIFIER ERROR DUE TO FINITE GAIN

The formula for the output of a summing amplifier, assuming negligible current flow to the amplifier, is given by Korn and Korn [6] as:

$$\frac{Eo}{E_{in}} = \frac{A}{(1 - A)\frac{R_1}{R_f} + 1}$$

where R_1 is the input resistor

R_f is the feedback resistor

A is the open loop gain = $-|A|$

Rearranging,

$$\frac{Eo}{E_{in}} = -\frac{R_f}{R_1}\left[\frac{1}{\frac{1}{|A|}\left(1 + \frac{R_f}{R_1}\right) + 1}\right]$$

Assume $R_f = R_1$. Then

$$\frac{E_o}{E_{in}} = -\frac{1}{\left(\frac{2}{|A|} + 1\right)}$$

For infinite open loop gain, $\frac{E_o}{E_{in}} = -1$

A .1% maximum error restricts

$$\frac{E_o}{E_{in}} \text{ to } .999 < \left|\frac{E_o}{E_{in}}\right| < 1.001$$

Using the larger value,

$$-1.001 = -\frac{1}{\left(\frac{2}{|A|} + 1\right)} \text{ giving } |A| = 2002$$

or $|A|_{db} = 20 \log 2002 = 66.2$ db